FIG.1
PRIOR ART

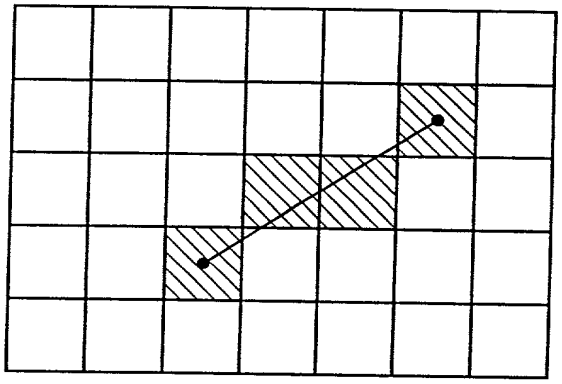


FIG.2A
PRIOR ART

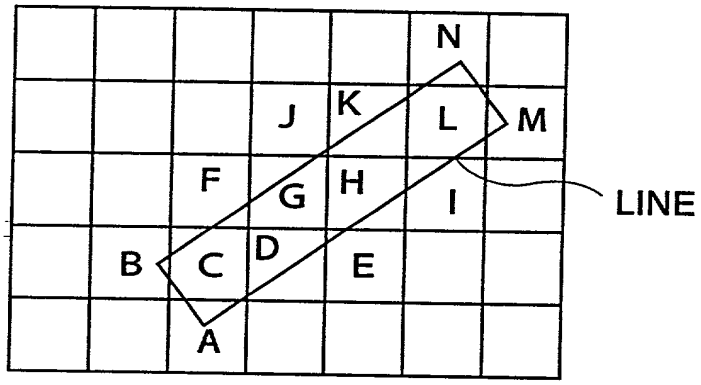


FIG.2B
PRIOR ART

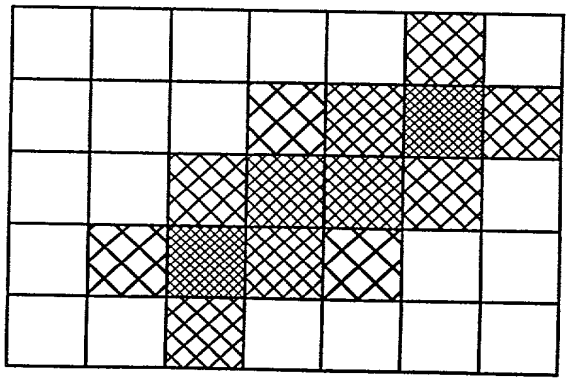
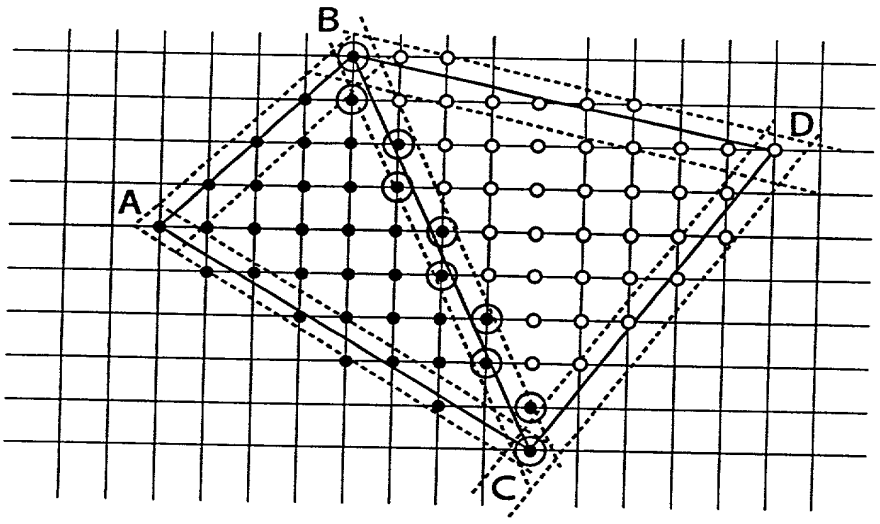


FIG.3
PRIOR ART



• :PIXELS WHEN TRIANGLE ABC IS DRAWN

o :PIXELS WHEN TRIANGLE BCD IS DRAWN

FIG.4

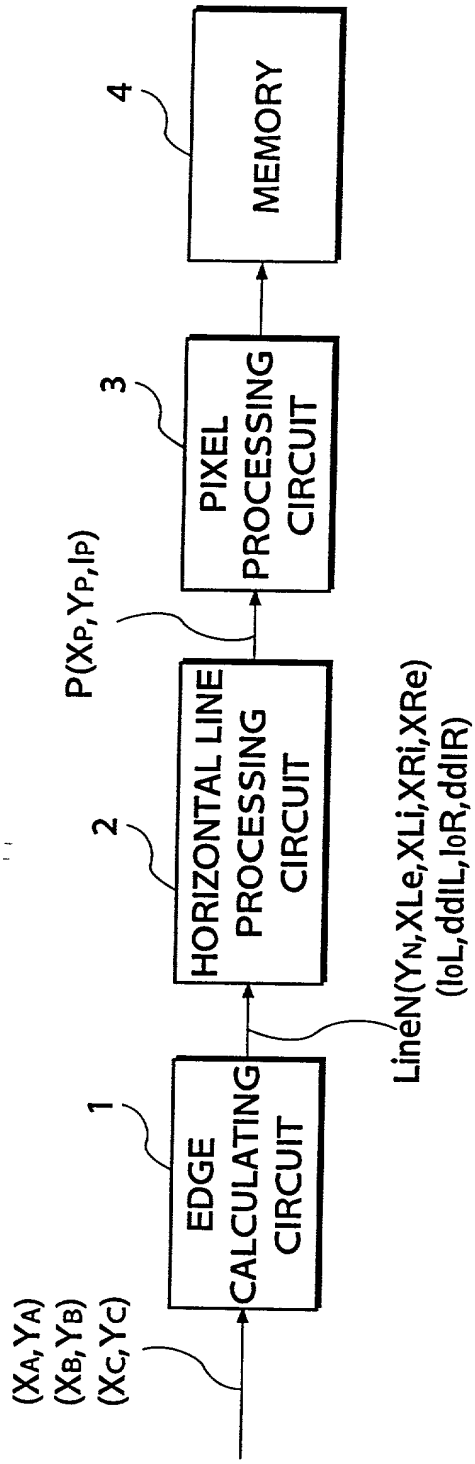

(XA,YA)
(XB,YB)
(XC,YC)
1
EDGE CALCULATING CIRCUIT
LineN(YN,XLe,XLi,XRi,XRe)
(IoL,ddIL,IoR,ddIR)
2
HORIZONTAL LINE PROCESSING CIRCUIT
P(XP,YP,IP)
3
PIXEL PROCESSING CIRCUIT
4
MEMORY

FIG.5

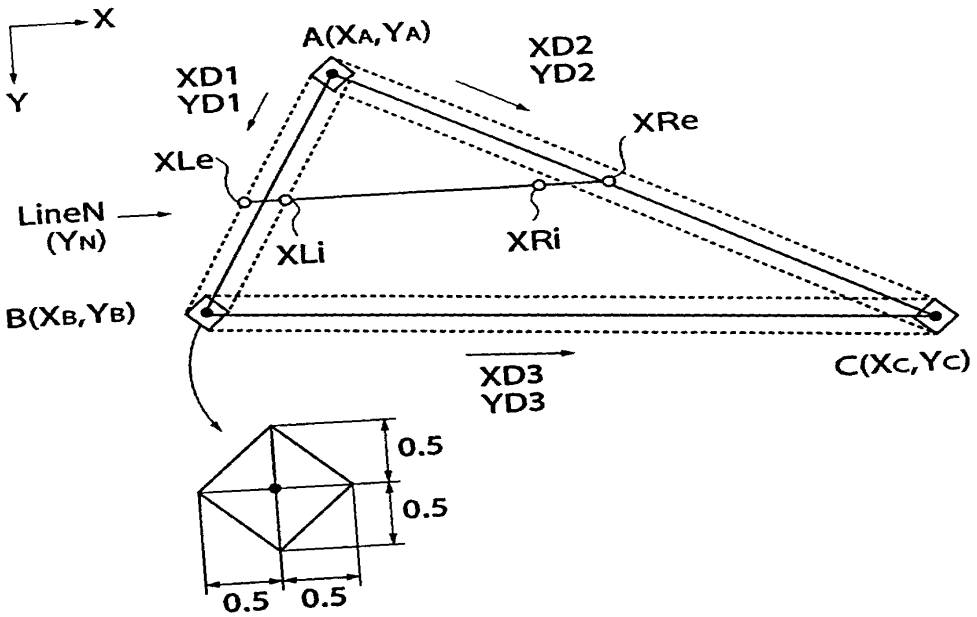

X
Y
A(XA,YA)
XD1
YD1
XD2
YD2
XRe
XLe
LineN
(YN)
XLi
XRi
B(XB,YB)
C(Xc,Yc)
XD3
YD3
0.5
0.5
0.5
0.5

FIG.6

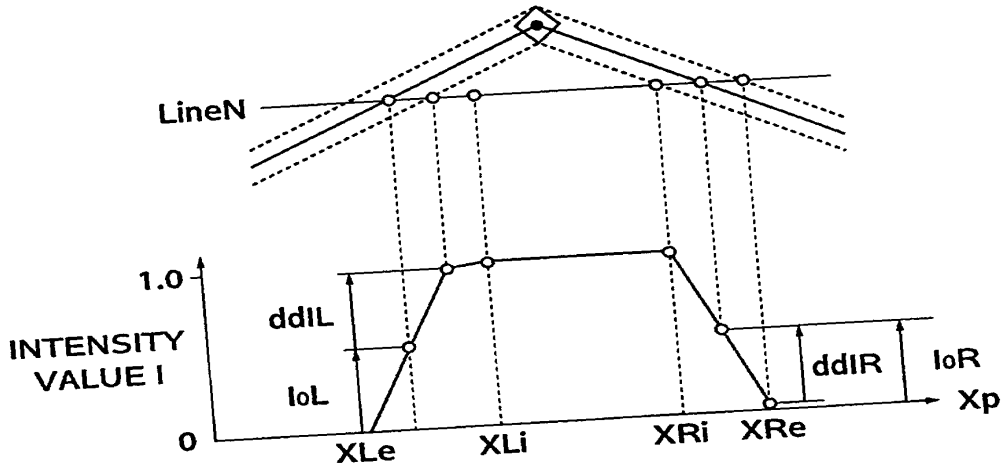

LineN
1.0
INTENSITY
VALUE I
0
ddIL
IoL
ddIR
IoR
Xp
XLe
XLi
XRi
XRe

FIG.7A

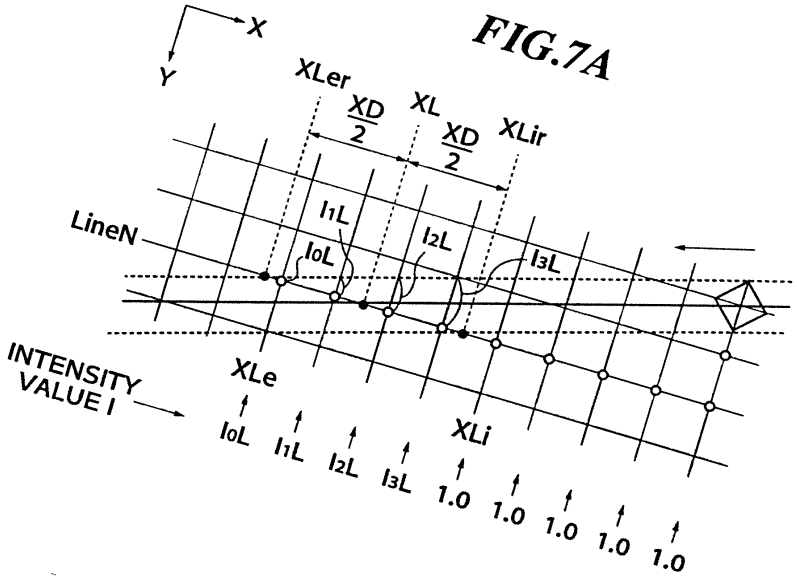

X
Y
XLer
XD/2
XL
XD/2
XLir
LineN
I1L
I0L
I2L
I3L
INTENSITY VALUE I
XLe
XLi
I0L I1L I2L I3L 1.0 1.0 1.0 1.0 1.0

FIG.7B

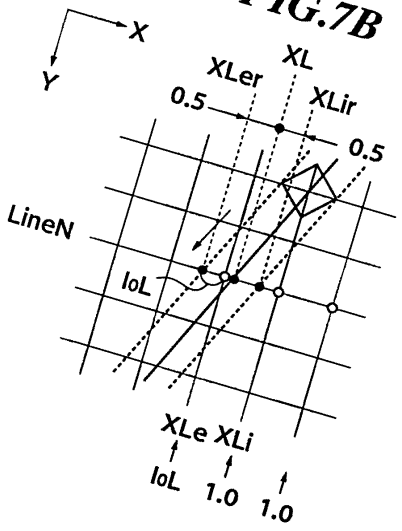

X
Y
XLer
XL
XLir
0.5
0.5
LineN
I0L
XLe XLi
I0L 1.0 1.0

FIG.8A

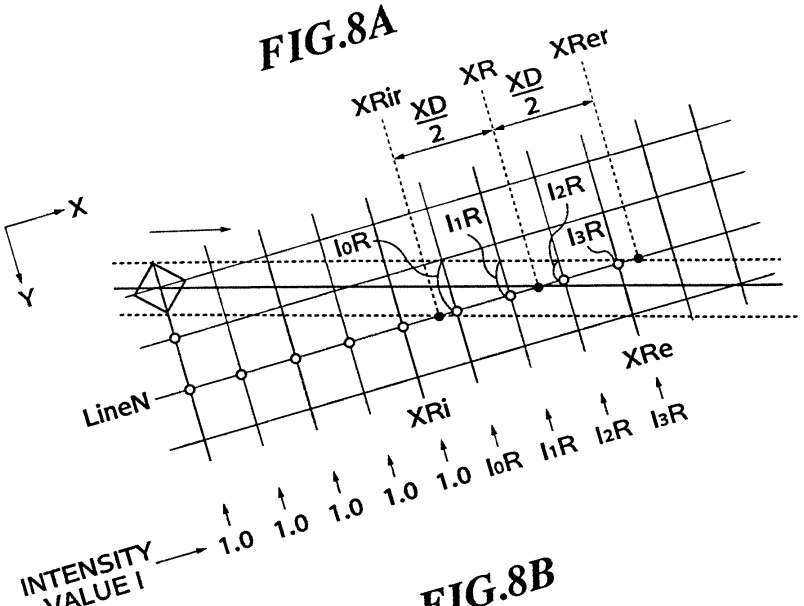

XRir
XD/2
XR
XD/2
XRer
X
Y
I0R
I1R
I2R
I3R
LineN
XRi
XRe
INTENSITY VALUE I
1.0 1.0 1.0 1.0 1.0 I0R I1R I2R I3R

FIG.8B

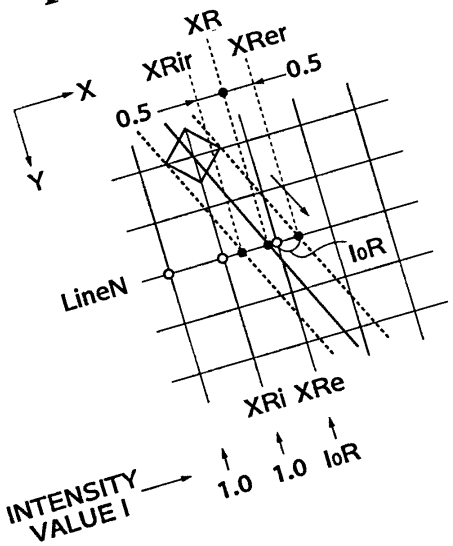

XR
XRir
XRer
0.5
0.5
X
Y
I0R
LineN
XRi XRe
INTENSITY VALUE I
1.0 1.0 I0R

FIG.9

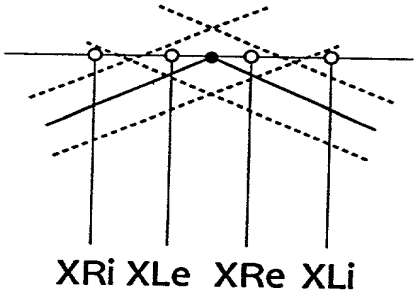


FIG.10

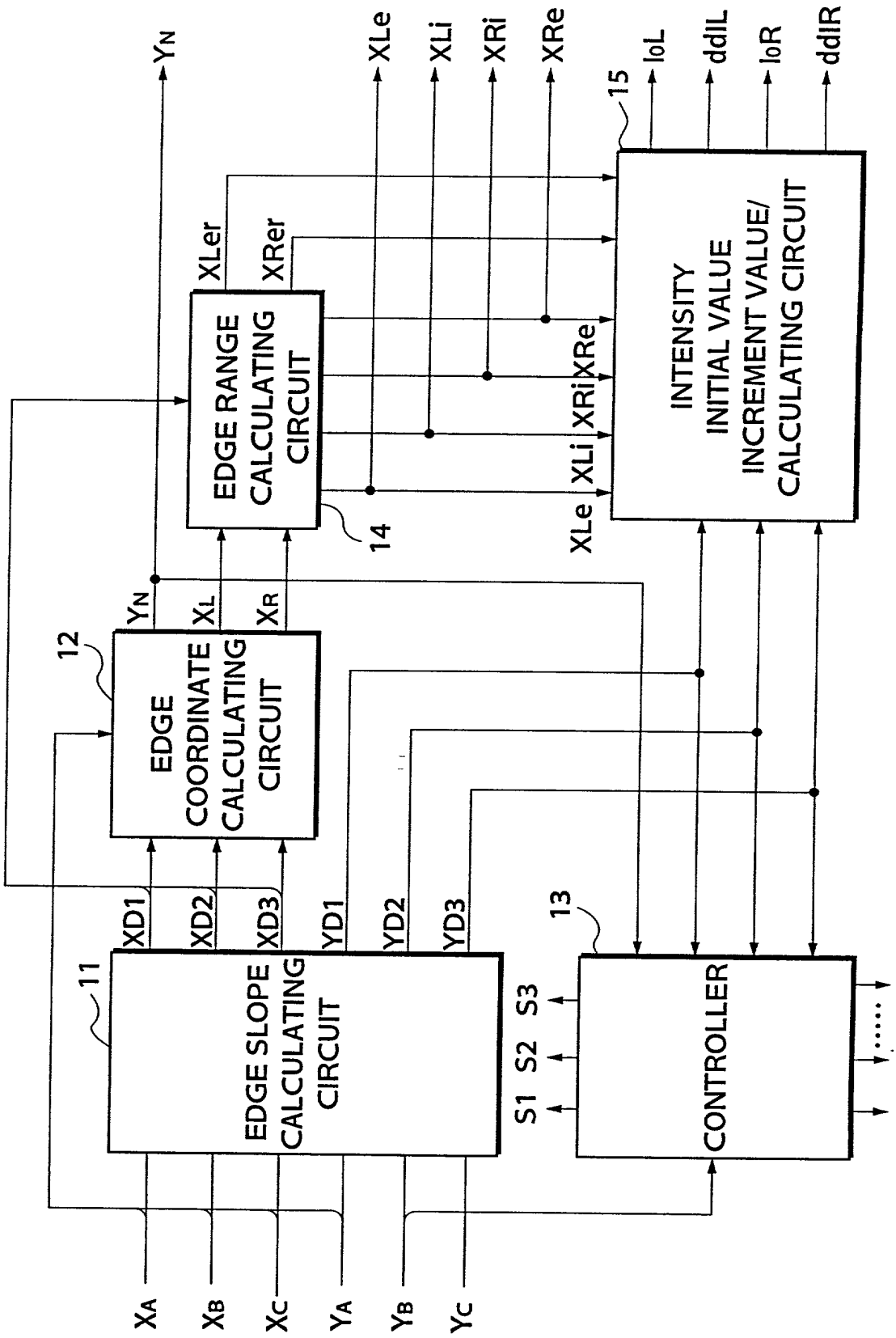

EDGE SLOPE CALCULATING CIRCUIT
11
EDGE COORDINATE CALCULATING CIRCUIT
12
CONTROLLER
13
EDGE RANGE CALCULATING CIRCUIT
14
INTENSITY INITIAL VALUE/ INCREMENT VALUE/ CALCULATING CIRCUIT
15
XA
XB
XC
YA
YB
YC
XD1
XD2
XD3
YD1
YD2
YD3
S1 S2 S3
YN
XL
XR
XLer
XRer
XLe
XLi
XRi
XRe
IoL
ddIL
IoR
ddIR

FIG.11

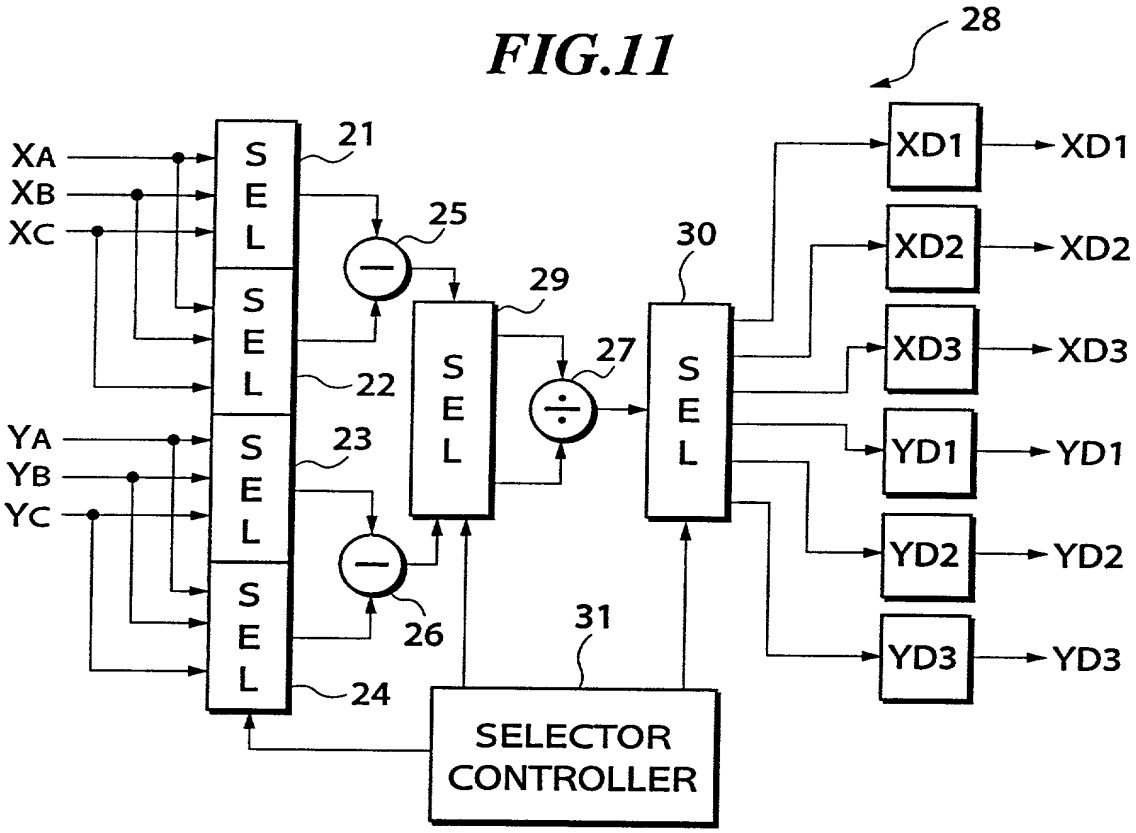

28
XA
XB
XC
YA
YB
YC
SEL
21
22
23
24
25
26
29
27
30
31
XD1
XD2
XD3
YD1
YD2
YD3
SELECTOR CONTROLLER

FIG.12

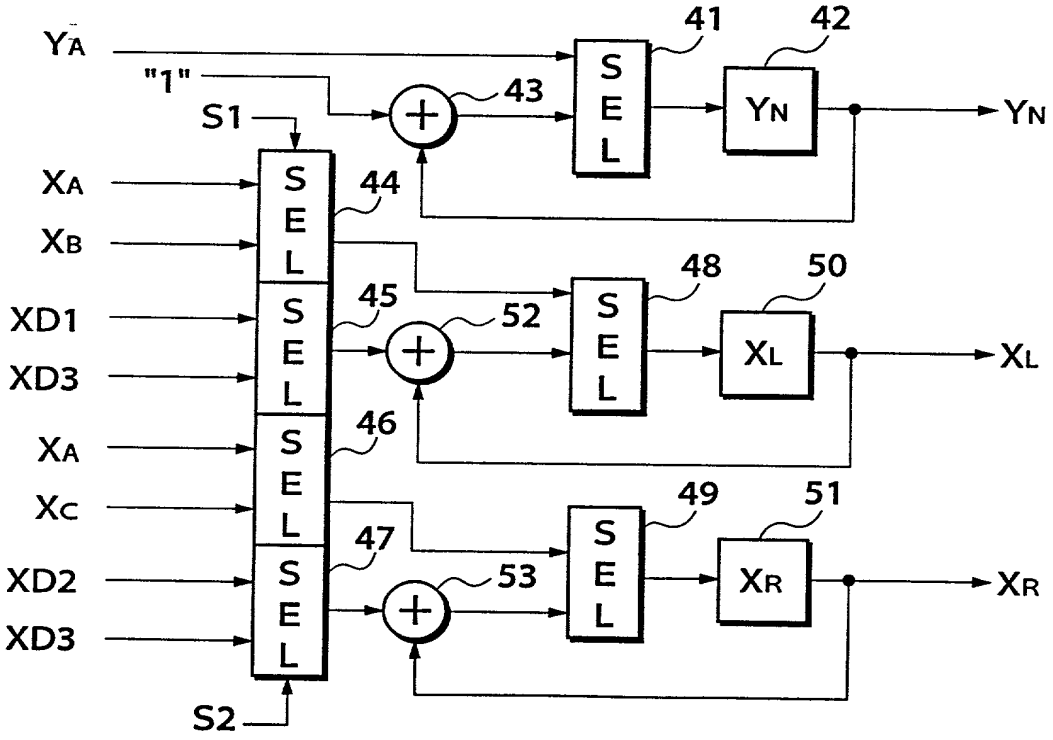

YA
"1"
S1
XA
XB
XD1
XD3
XA
XC
XD2
XD3
S2
SEL
41
42
43
YN
44
45
46
47
48
50
52
XL
49
51
53
XR

FIG.13

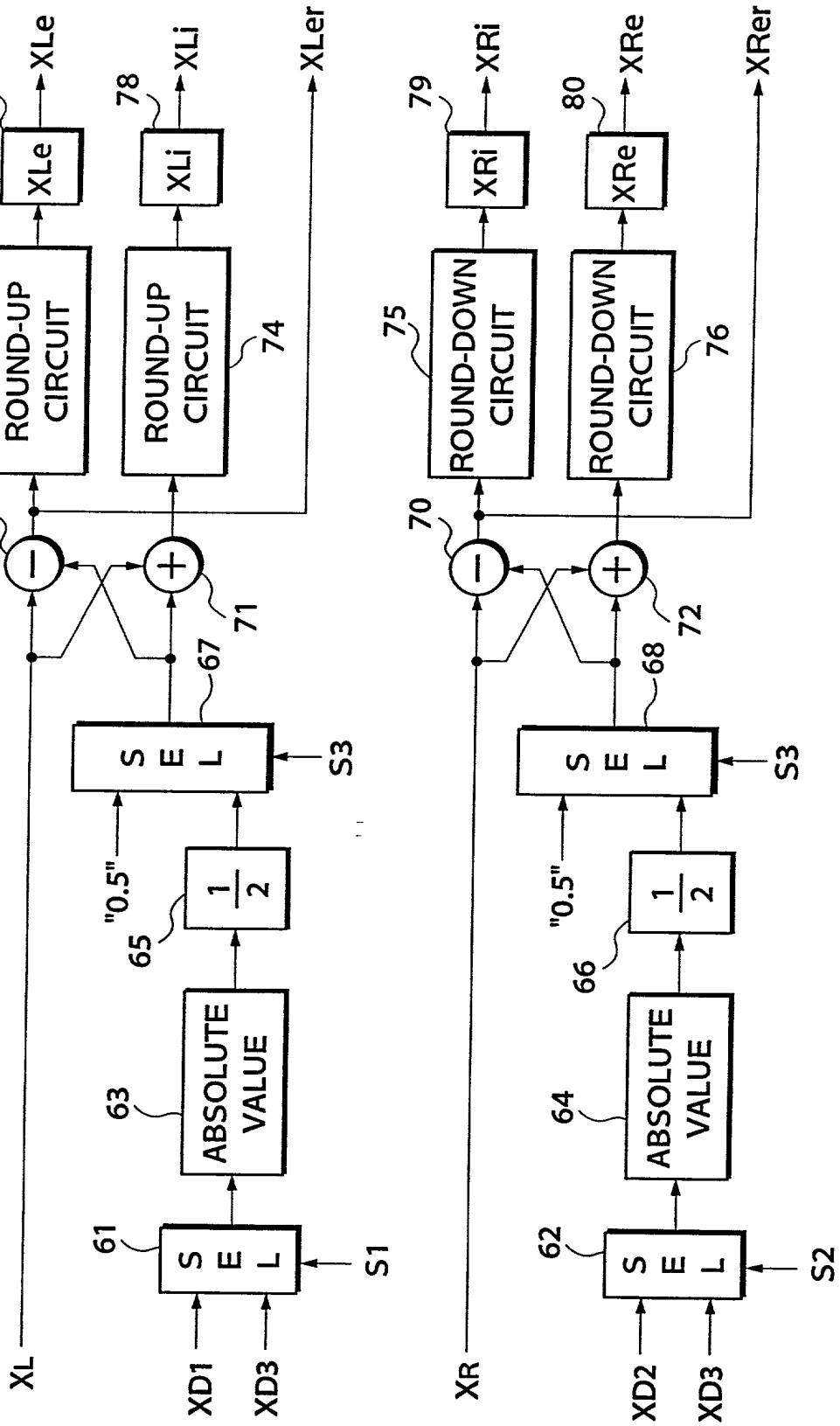

XL
XD1
XD3
S1
S2
S3
SEL
61
62
63
64
ABSOLUTE VALUE
65
66
"0.5"
1/2
67
68
69
70
71
72
73
74
75
76
77
78
79
80
ROUND-UP CIRCUIT
ROUND-DOWN CIRCUIT
XLe
XLi
XLer
XRi
XRe
XRer
XR
XD2

FIG.14

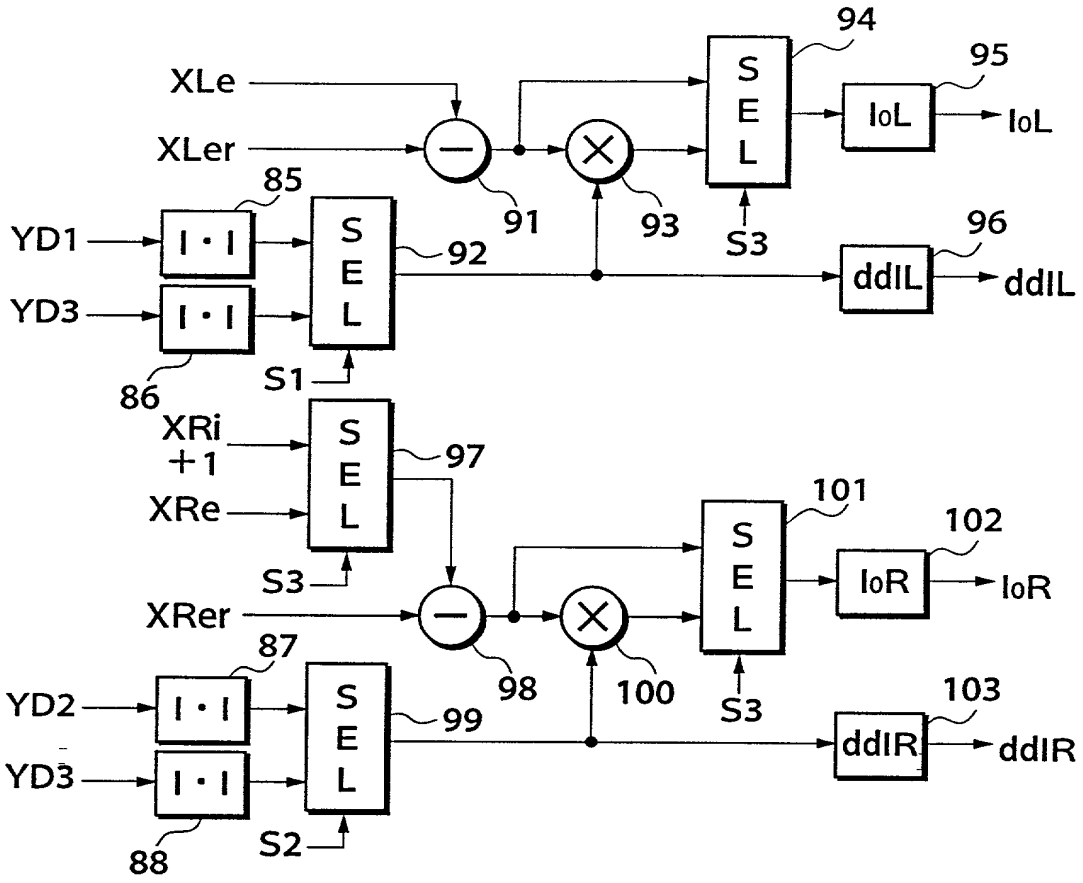

XLe
XLer
YD1
YD3
YD2
YD3
XRi +1
XRe
XRer
I・I
SEL
91
92
93
94
95
96
97
98
99
100
101
102
103
85
86
87
88
S1
S2
S3
IoL
ddIL
IoR
ddIR

FIG.15A

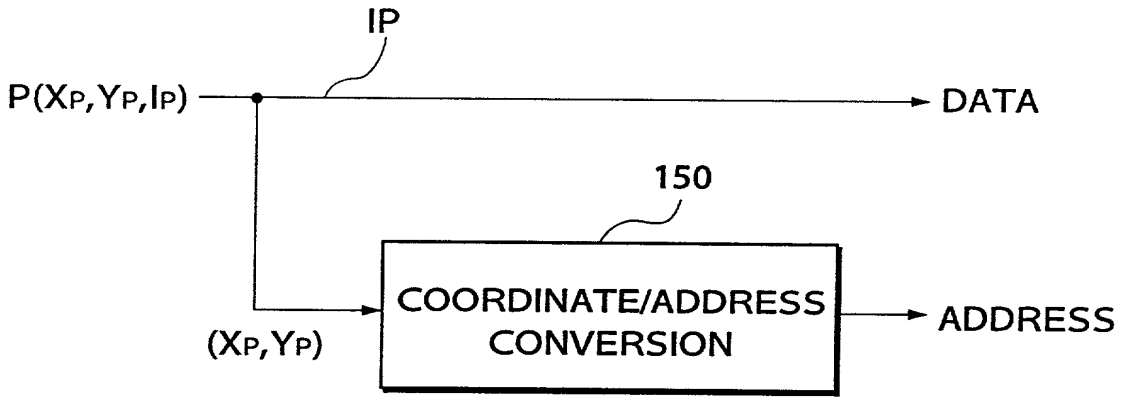

IP
P(XP,YP,IP)
DATA
150
COORDINATE/ADDRESS CONVERSION
ADDRESS
(XP,YP)

FIG.15B

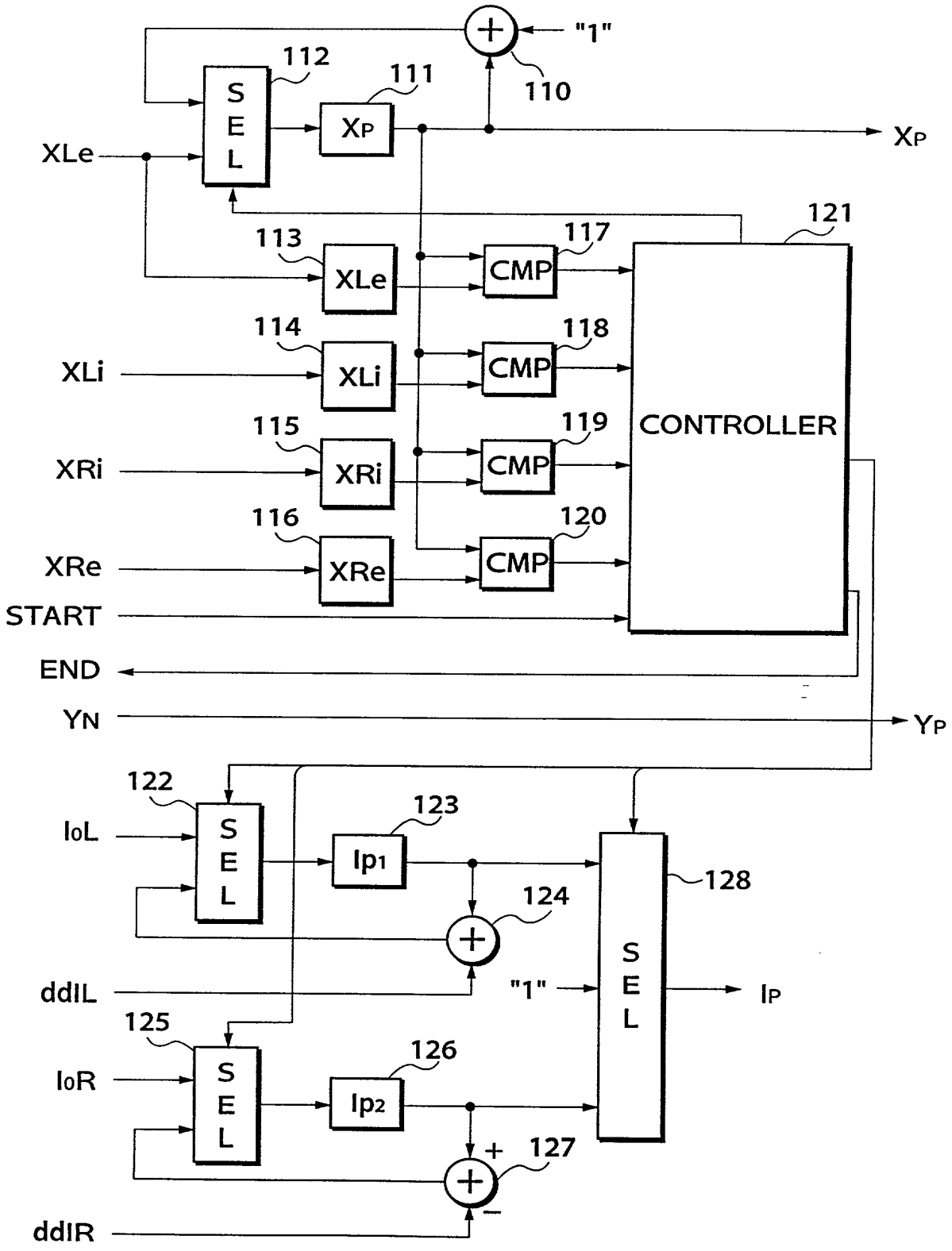

"1"
110
112
111
SEL
XP
XLe
XP
121
113
117
XLe
CMP
114
118
XLi
XLi
CMP
CONTROLLER
115
119
XRi
XRi
CMP
116
120
XRe
XRe
CMP
START
END
YN
YP
122
123
IoL
SEL
Ip1
128
124
"1"
ddIL
SEL
IP
125
126
IoR
SEL
Ip2
+
127
−
ddIR

FIG.16

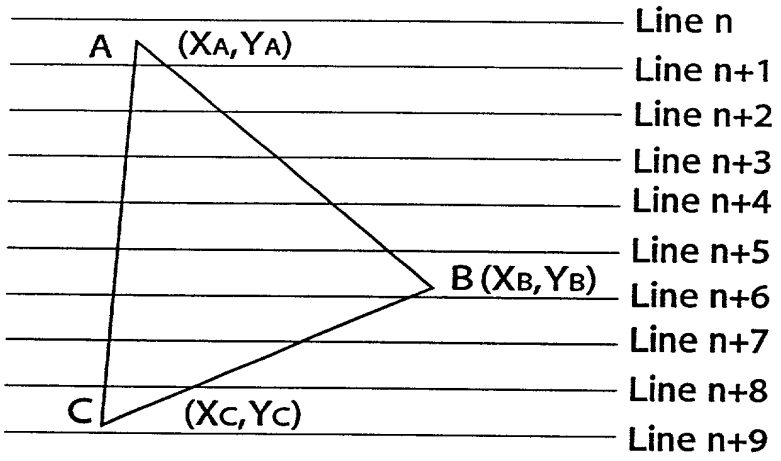


FIG.17

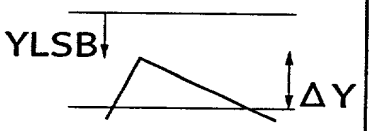
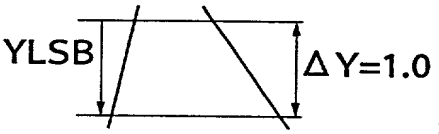
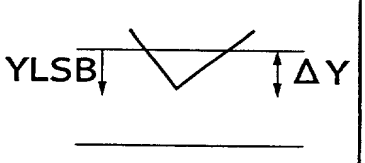
PATTERN A	PATTERN B	PATTERN C
		

FIG.18

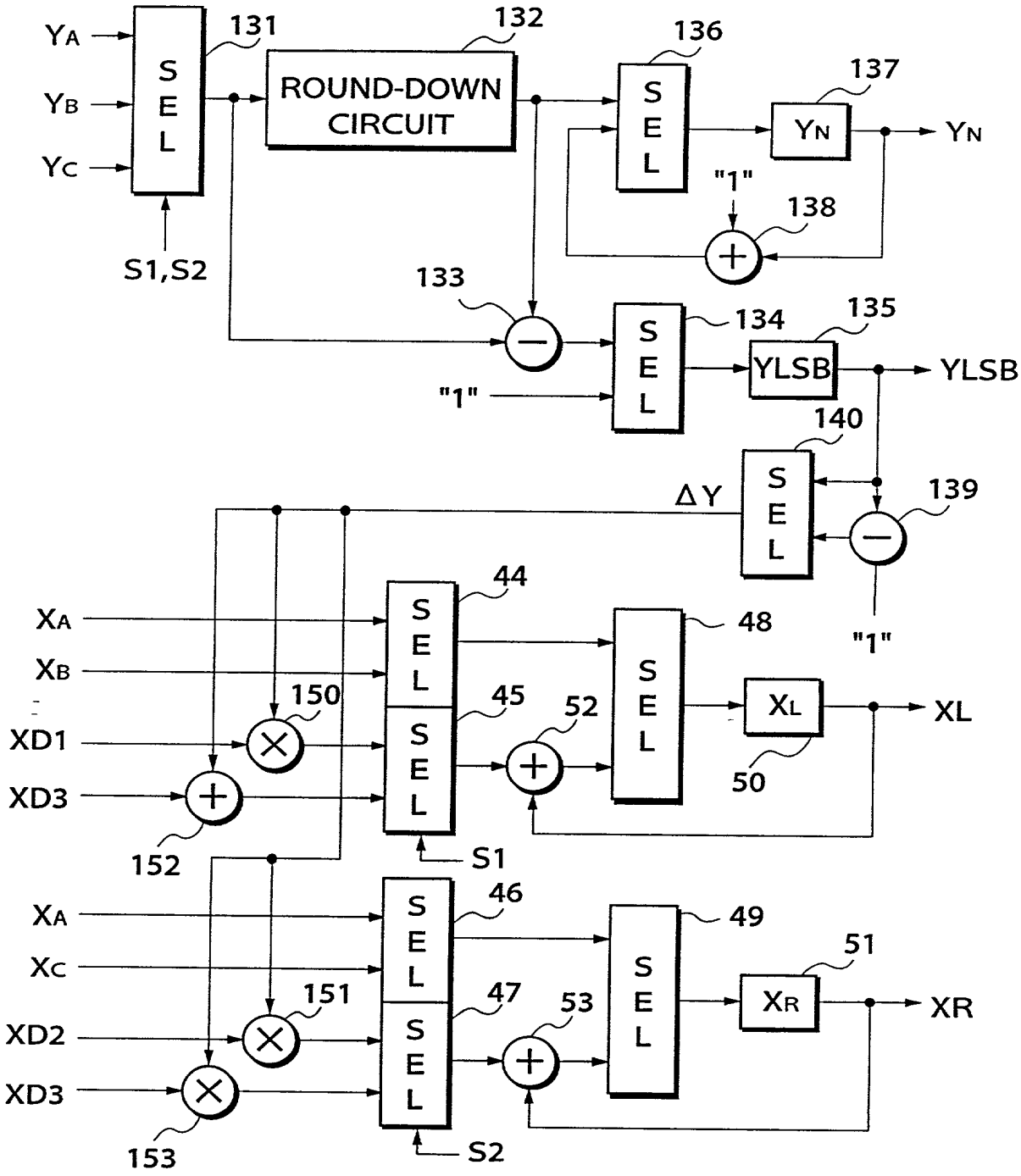

YA
YB
YC
SEL
131
S1,S2
ROUND-DOWN CIRCUIT
132
136
137
YN
YN
"1"
138
133
134
135
YLSB
YLSB
"1"
140
ΔY
139
"1"
XA
XB
XD1
XD3
150
152
44
45
52
48
XL
XL
50
S1
XA
XC
XD2
XD3
151
153
46
47
53
49
51
XR
XR
S2

FIG.19

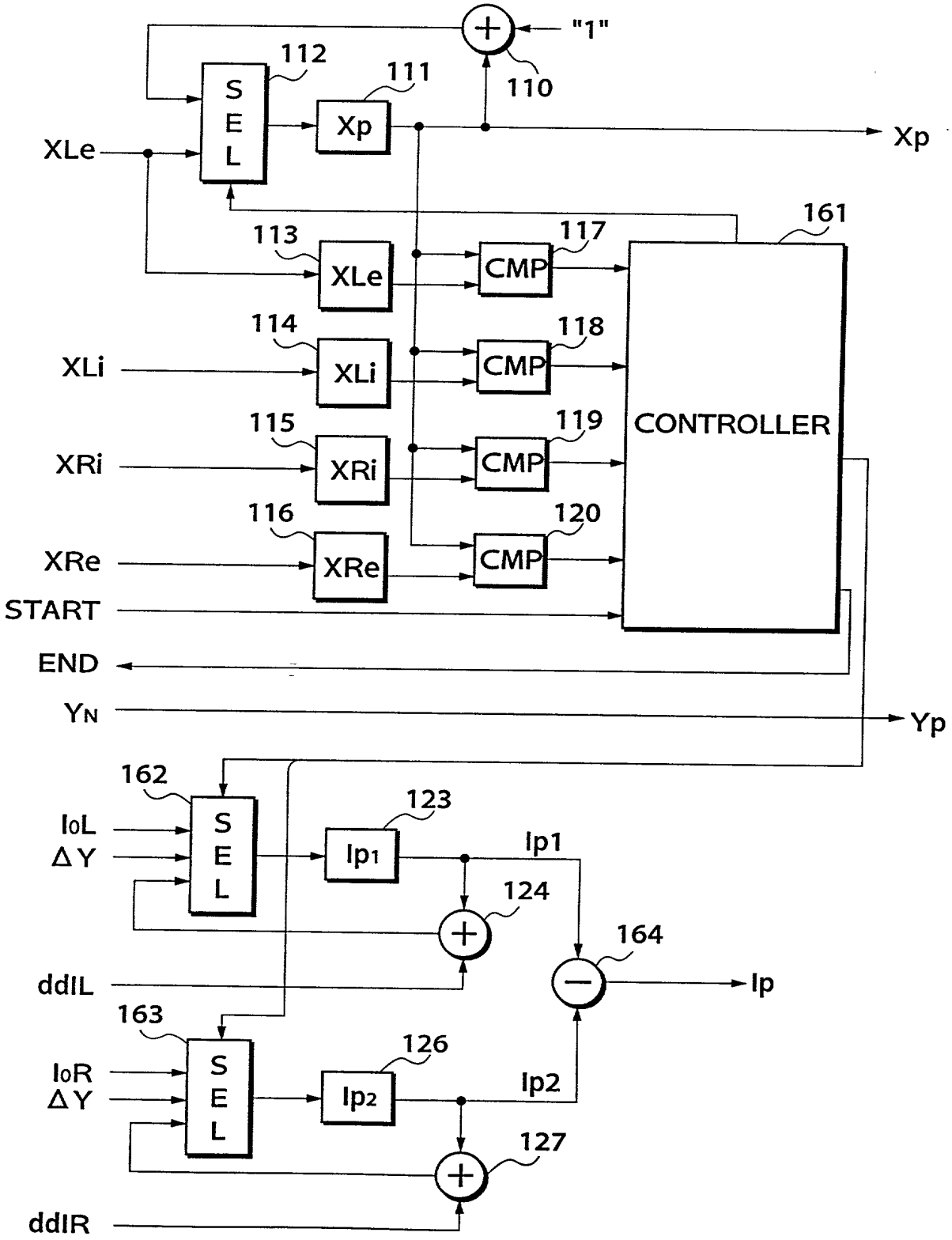

"1"
110
112
111
S
E
L
Xp
XLe
Xp
161
113
117
XLe
CMP
114
118
XLi
XLi
CMP
CONTROLLER
115
119
XRi
XRi
CMP
116
120
XRe
XRe
CMP
START
END
YN
Yp
162
123
IoL
ΔY
S
E
L
Ip1
Ip1
124
164
ddIL
Ip
163
126
IoR
ΔY
S
E
L
Ip2
Ip2
127
ddIR

FIG.20

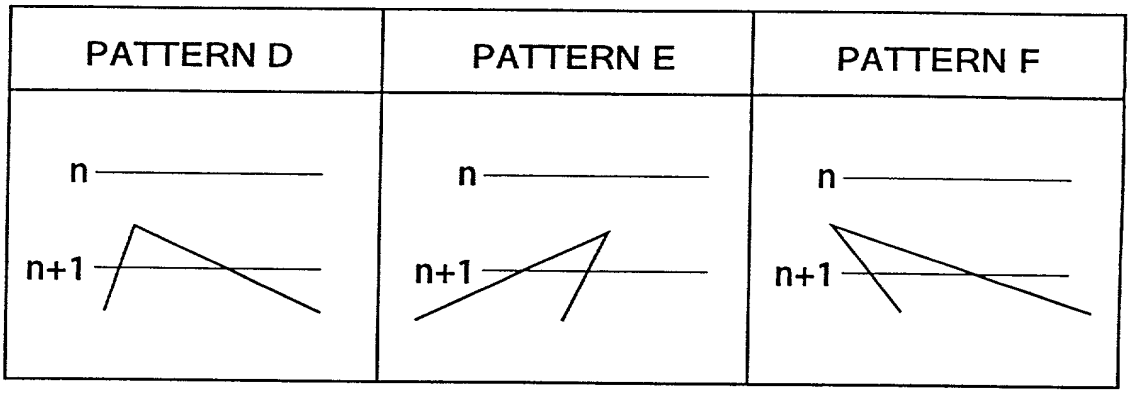


FIG.21A

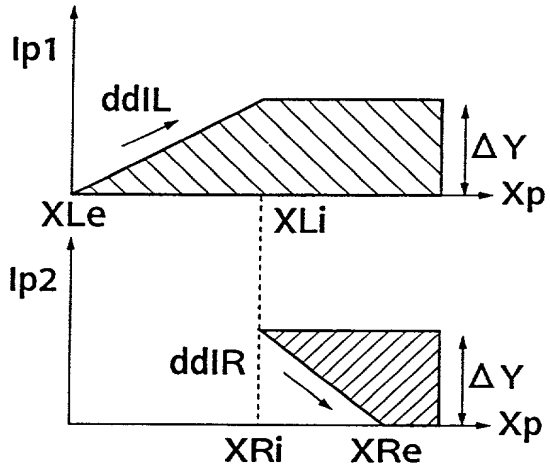


FIG.21B

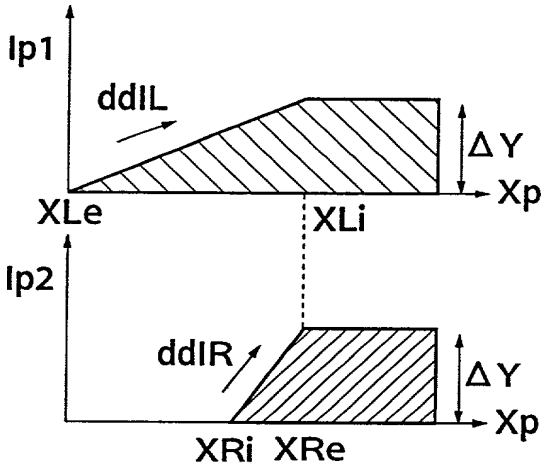


FIG.21C

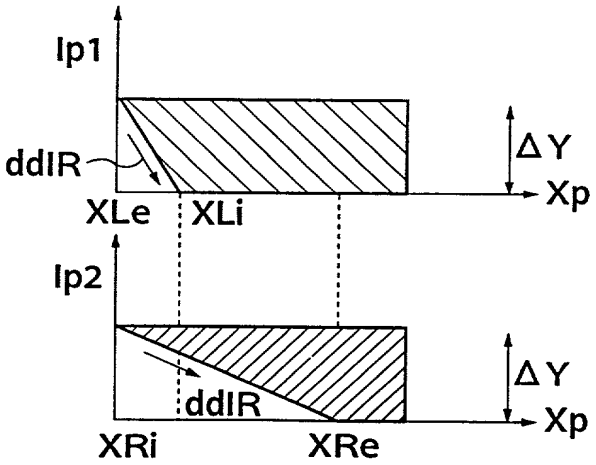


FIG.22A

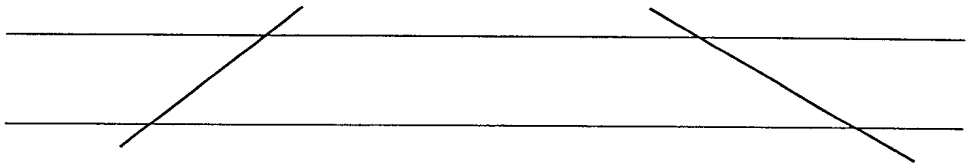


FIG.22B

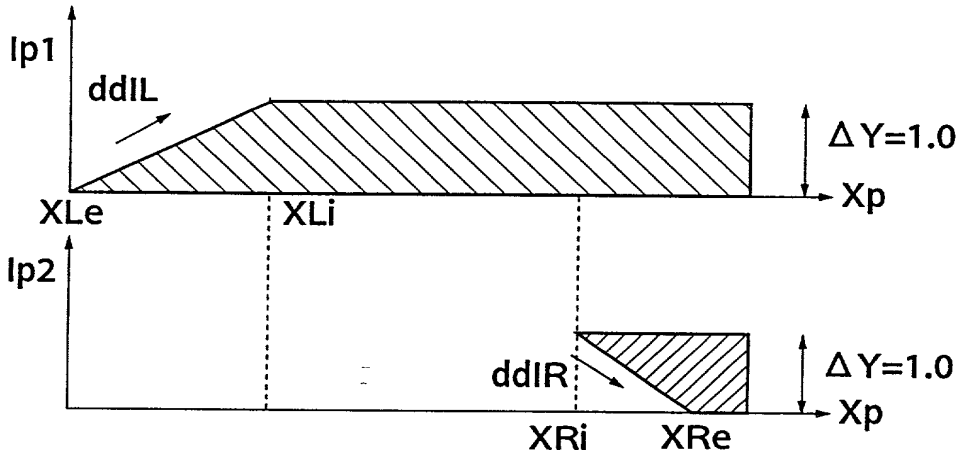


FIG.23

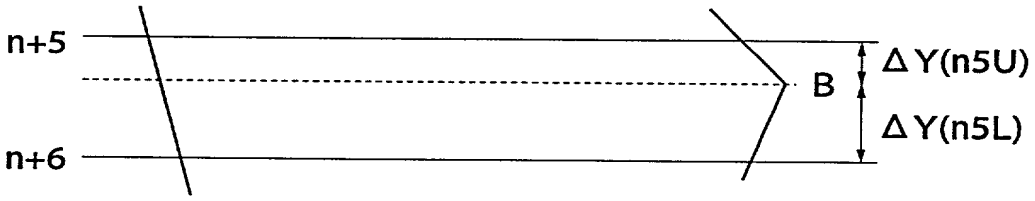


FIG.24A

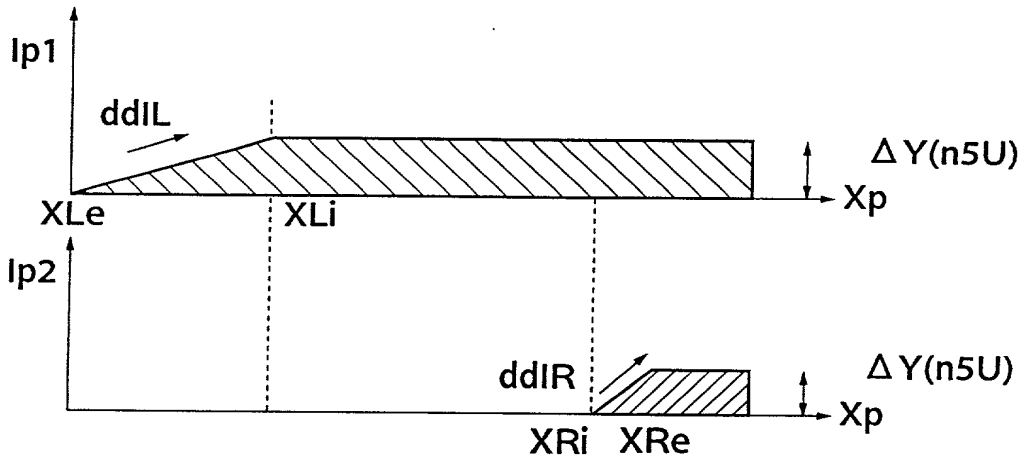


FIG.24B

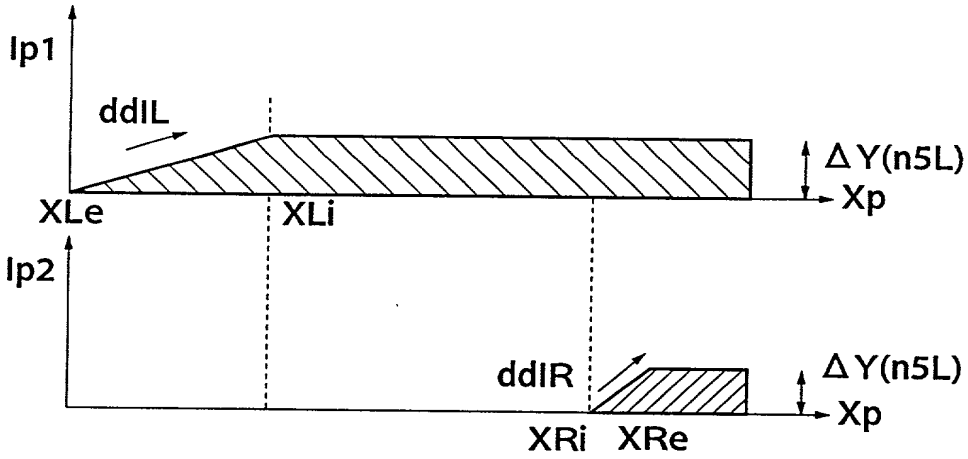


FIG.25

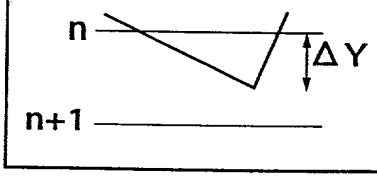
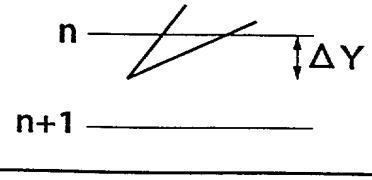
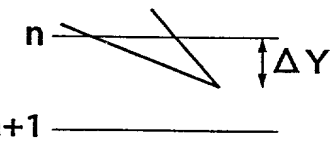
PATTERN G	PATTERN H	PATTERN I
		

FIG.26

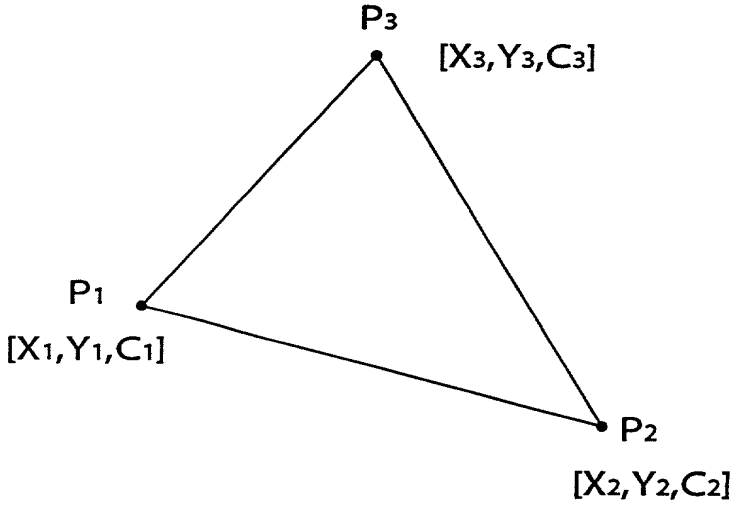


FIG.27A

1.Move [X1,Y1,C1]

2.Move [X2,Y2,C2]

3.Triangle_Fill [X3,Y3,C3]

4.Triangle_Fill [X4,Y4,C4]

5.Triangle_Fill [X5,Y5,C5]

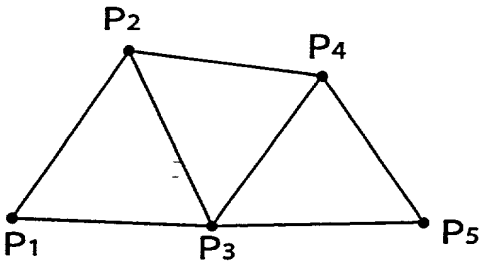


FIG.27B

1.Move [X1,Y1,C1]

2.Move [X2,Y2,C2]

3.Triangle_Fill [X3,Y3,C3]

4.Triangle_Fill [X4,Y4,C4]

5.Triangle_Fill [X5,Y5,C5]

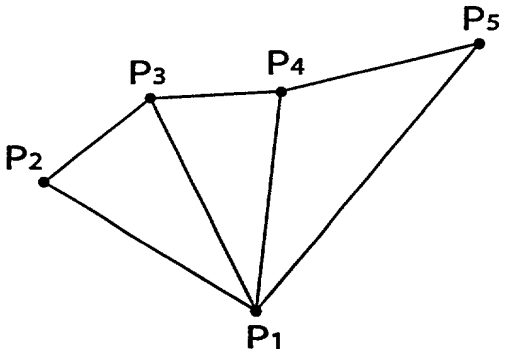


FIG.28

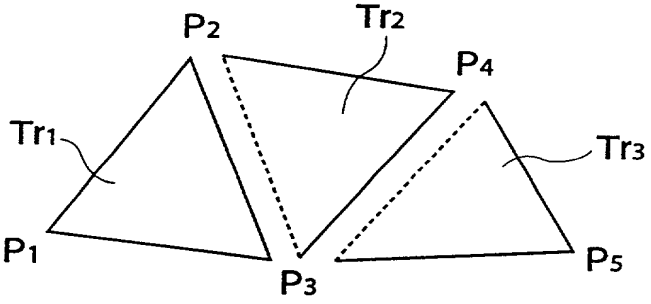


FIG.29

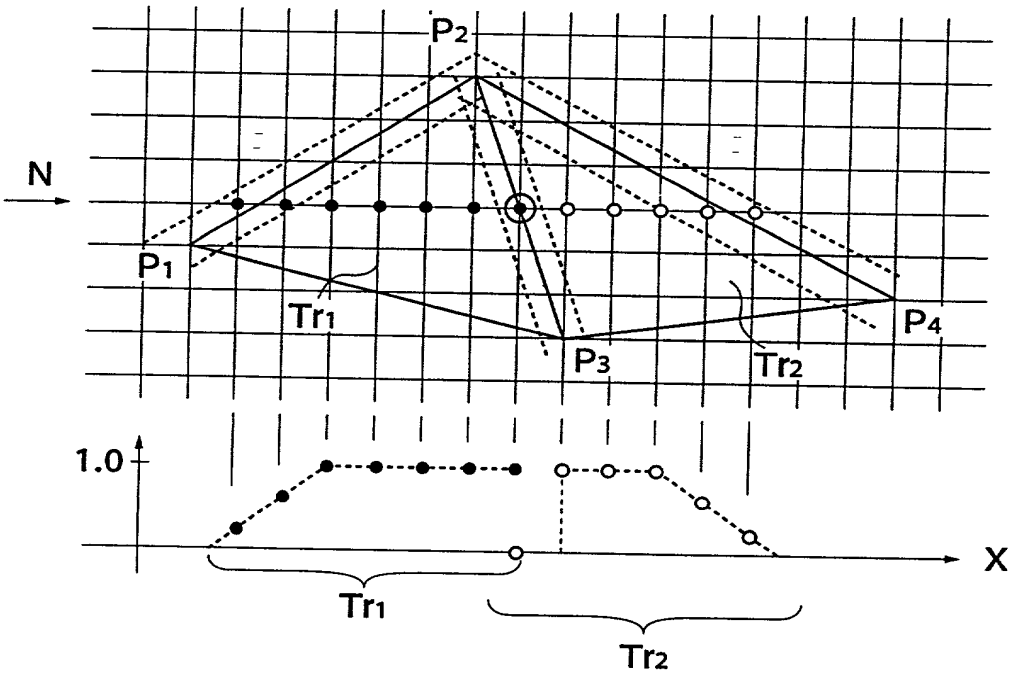
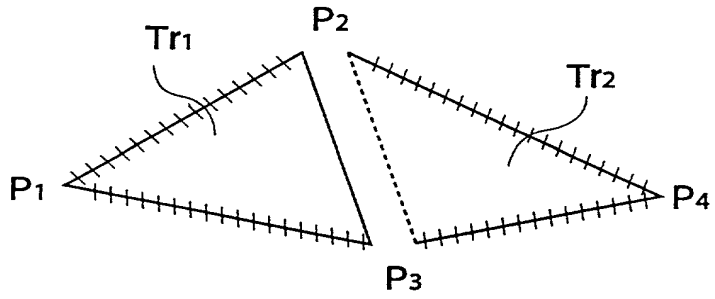


FIG.30

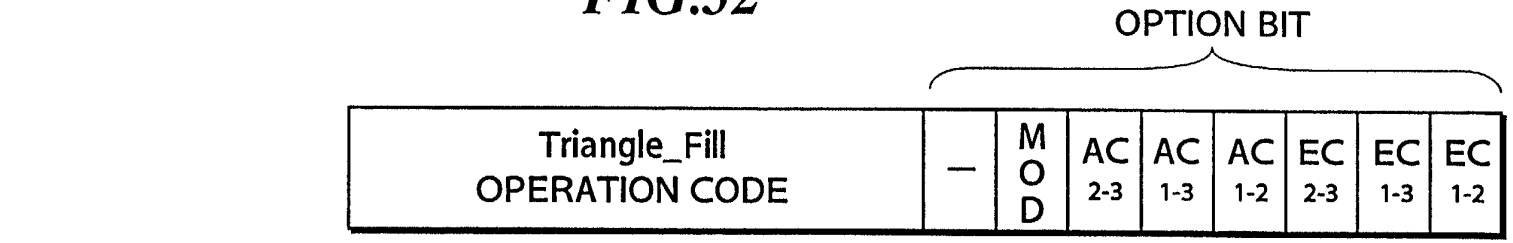


++++++++	EDGE WHICH IS SUBJECTED TO INTENSITY PROCESSING
————	EDGE WHICH IS DRAWN BUT NOT SUBJECTED TO INTENSITY PROCESSING
----------	EDGE WHICH IS NOT DRAWN

FIG.31

Move [X_1,Y_1,C_1]	OPERATION CODE | OPTION BIT X_1 COORDINATE Y_1 COORDINATE C_1 DATA
Move [X_2,Y_2,C_2]	OPERATION CODE | OPTION BIT X_2 COORDINATE Y_2 COORDINATE C_2 DATA
Triangle_Fill [X_3,Y_3,C_3]	OPERATION CODE | OPTION BIT X_3 COORDINATE Y_3 COORDINATE C_3 DATA

FIG.32



MOD; 0 STRIP MODE
1 FAN MODE

AC_{1-2}; 0 NO INTENSITY PROCESSING IS PERFORMED ON EDGE P_1-P_2
1 INTENSITY PROCESSING IS PERFORMED ON EDGE P_1-P_2

AC_{1-3}; 0 NO INTENSITY PROCESSING IS PERFORMED ON EDGE P_1-P_3
1 INTENSITY PROCESSING IS PERFORMED ON EDGE P_1-P_3

AC_{2-3}; 0 NO INTENSITY PROCESSING IS PERFORMED ON EDGE P_2-P_3
1 INTENSITY PROCESSING IS PERFORMED ON EDGE P_2-P_3

EC_{1-2}; 0 EDGE P_1-P_2 IS DRAWN
1 EDGE P_1-P_2 IS NOT DRAWN

EC_{1-3}; 0 EDGE P_1-P_3 IS DRAWN
1 EDGE P_1-P_3 IS NOT DRAWN

EC_{2-3}; 0 EDGE P_2-P_3 IS DRAWN
1 EDGE P_2-P_3 IS NOT DRAWN

FIG.33A

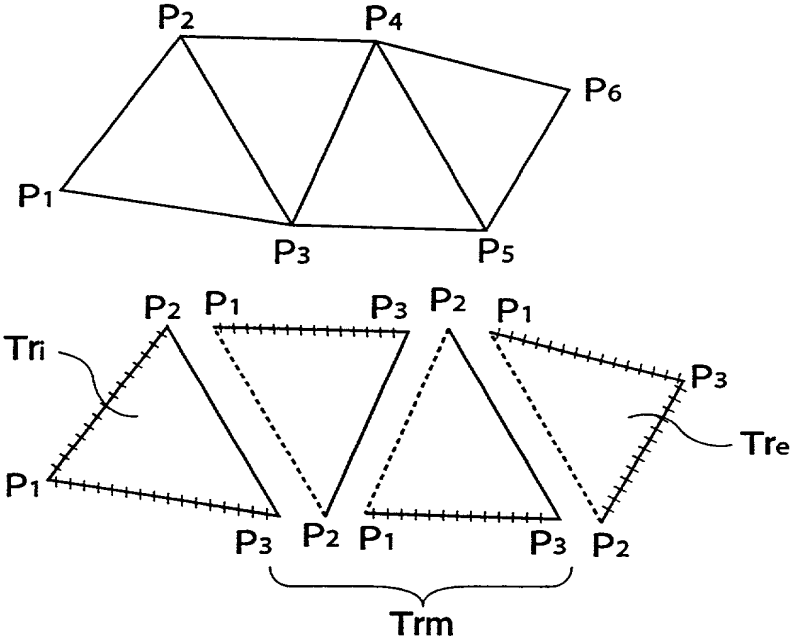


FIG.33B

OPTION BIT	MOD	AC 2-3	AC 1-3	AC 1-2	EC 2-3	EC 1-3	EC 1-2
Tri	0	0	1	1	0	0	0
Trm	0	0	1	0	0	0	1
Tre	0	1	1	0	0	0	1

FIG.34A

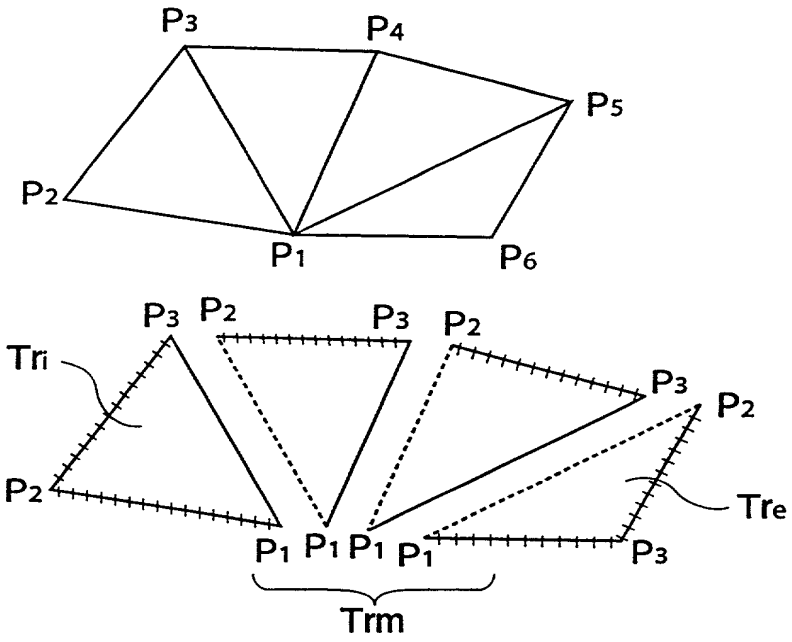


FIG.34B

OPTION BIT	MOD	AC 2-3	AC 1-3	AC 1-2	EC 2-3	EC 1-3	EC 1-2
Tri	0	1	0	1	0	0	0
Trm	1	1	0	0	0	0	1
Tre	1	1	1	0	0	0	1

FIG.35

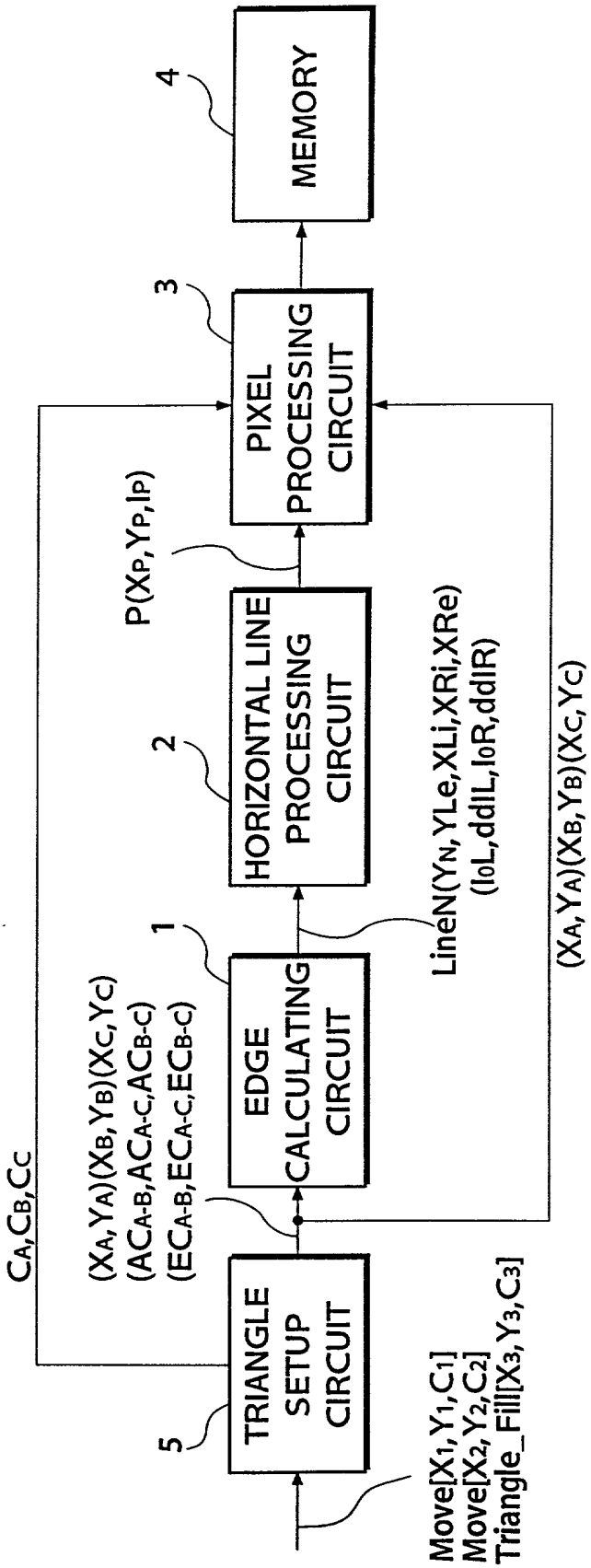

MEMORY
4
PIXEL PROCESSING CIRCUIT
3
HORIZONTAL LINE PROCESSING CIRCUIT
2
EDGE CALCULATING CIRCUIT
1
TRIANGLE SETUP CIRCUIT
5
P(XP,YP,IP)
LineN(YN,YLe,XLi,XRi,XRe)
(I0L,ddIL,I0R,ddIR)
(XA,YA)(XB,YB)(XC,YC)
CA,CB,CC
(XA,YA)(XB,YB)(XC,YC)
(ACA-B,ACA-C,ACB-C)
(ECA-B,ECA-C,ECB-C)
Move[X1,Y1,C1]
Move[X2,Y2,C2]
Triangle_Fill[X3,Y3,C3]

FIG.36

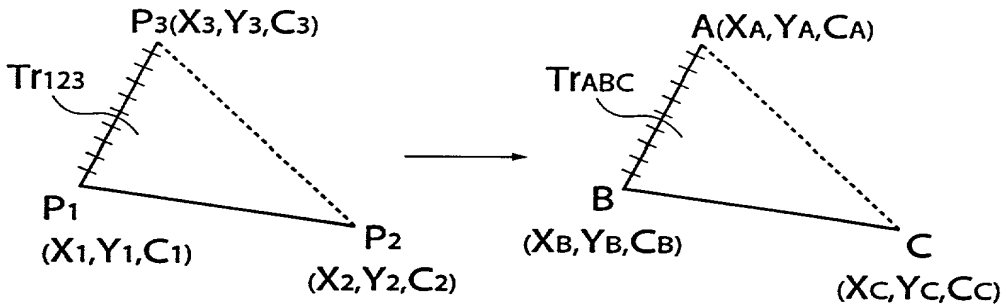
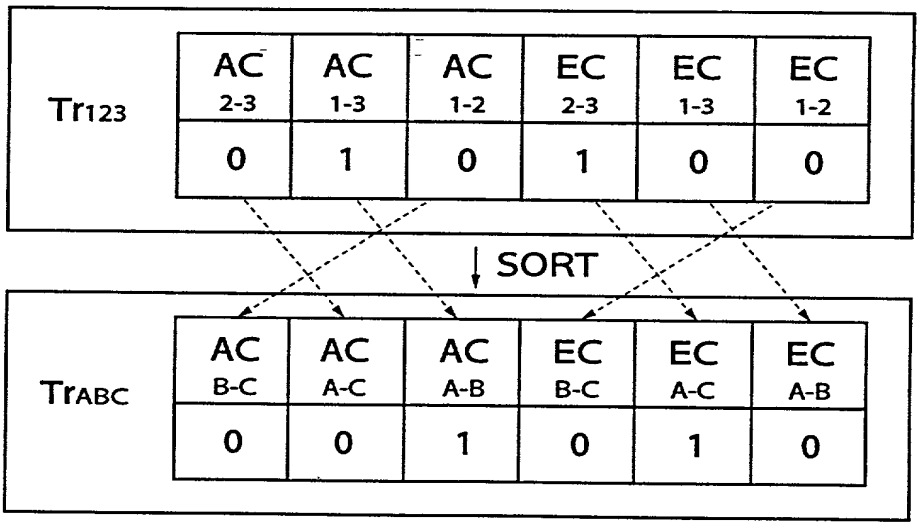

P3(X3,Y3,C3)
Tr123
P1
(X1,Y1,C1)
P2
(X2,Y2,C2)
A(XA,YA,CA)
TrABC
B
(XB,YB,CB)
C
(XC,YC,CC)

FIG.37


Tr123
AC 2-3
AC 1-3
AC 1-2
EC 2-3
EC 1-3
EC 1-2
0
1
0
1
0
0
SORT
TrABC
AC B-C
AC A-C
AC A-B
EC B-C
EC A-C
EC A-B
0
0
1
0
1
0

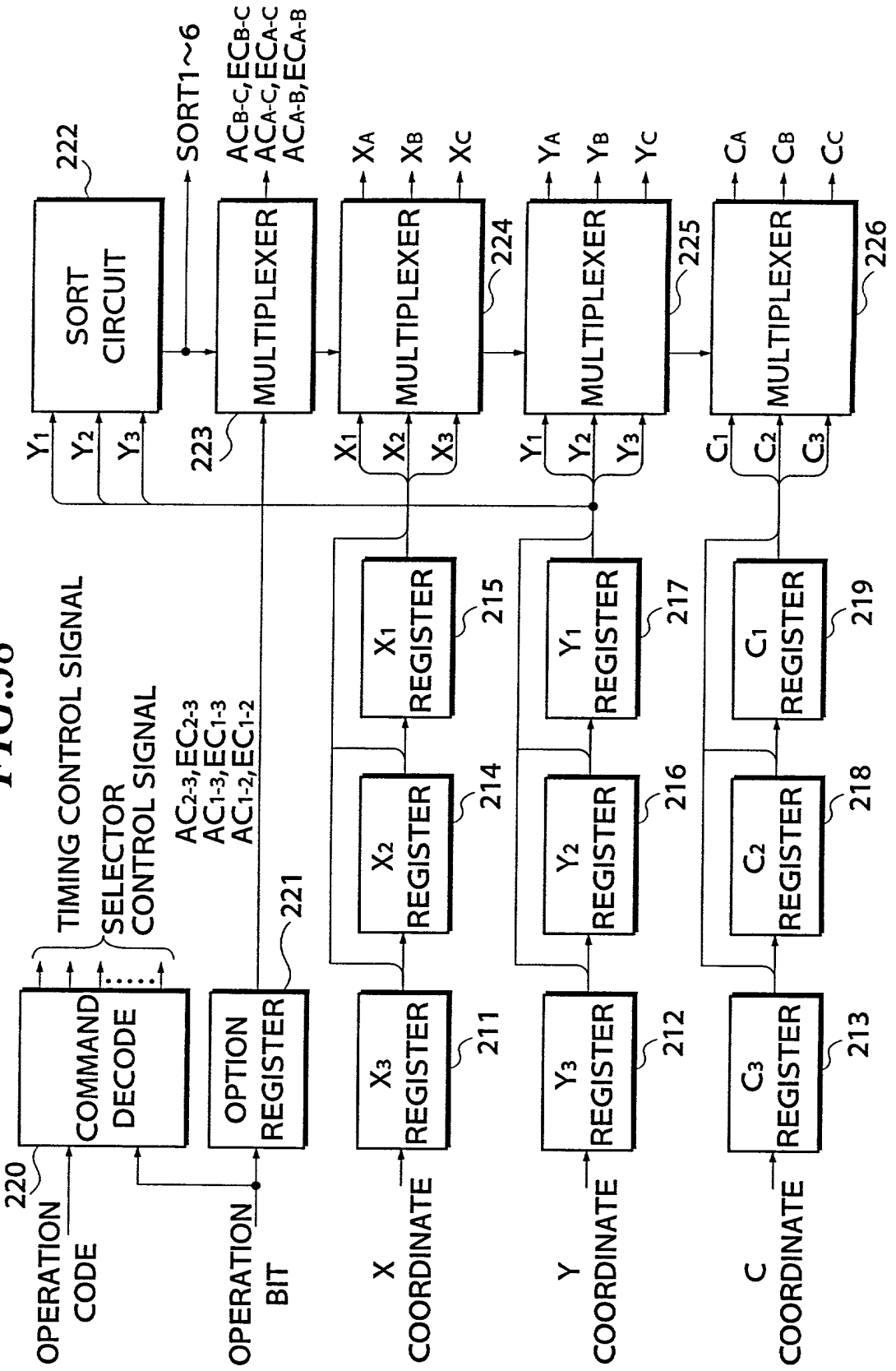

OPERATION CODE
220
COMMAND DECODE
TIMING CONTROL SIGNAL
SELECTOR CONTROL SIGNAL
OPERATION BIT
OPTION REGISTER
221
AC2-3,EC2-3
AC1-3,EC1-3
AC1-2,EC1-2
X COORDINATE
X3 REGISTER
211
X2 REGISTER
214
X1 REGISTER
215
Y COORDINATE
Y3 REGISTER
212
Y2 REGISTER
216
Y1 REGISTER
217
C COORDINATE
C3 REGISTER
213
C2 REGISTER
218
C1 REGISTER
219
SORT CIRCUIT
222
SORT1~6
MULTIPLEXER
223
ACB-C,ECB-C
ACA-C,ECA-C
ACA-B,ECA-B
MULTIPLEXER
224
XA XB XC
MULTIPLEXER
225
YA YB YC
MULTIPLEXER
226
CA CB CC
Y1 Y2 Y3
X1 X2 X3
Y1 Y2 Y3
C1 C2 C3

FIG.38

FIG.39

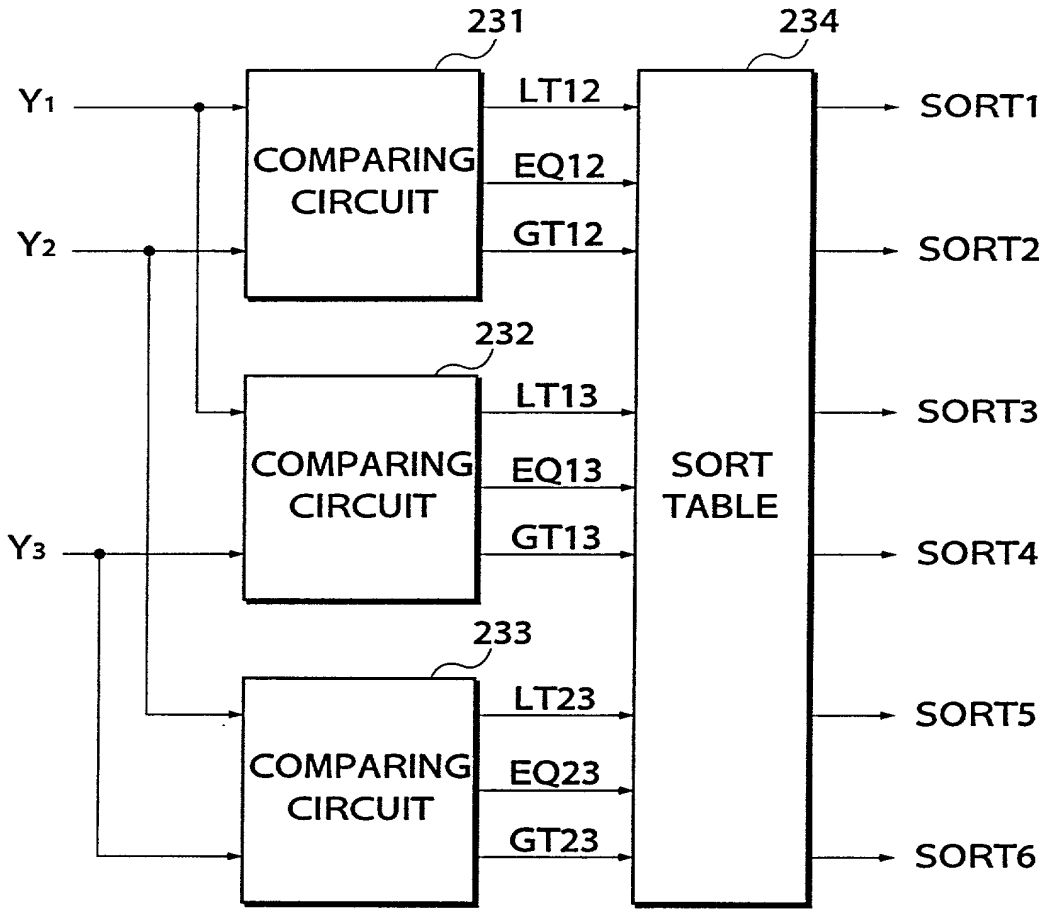

231
234
Y1
Y2
Y3
COMPARING CIRCUIT
LT12
EQ12
GT12
232
COMPARING CIRCUIT
LT13
EQ13
GT13
233
COMPARING CIRCUIT
LT23
EQ23
GT23
SORT TABLE
SORT1
SORT2
SORT3
SORT4
SORT5
SORT6

FIG.40

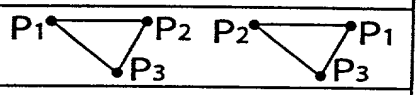
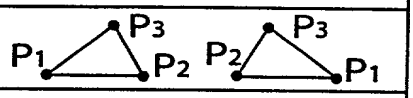
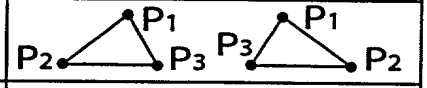
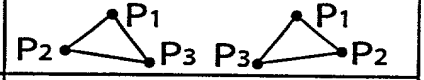
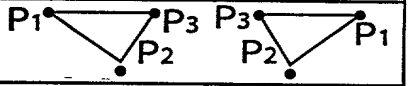
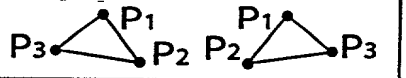
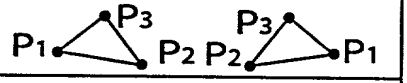
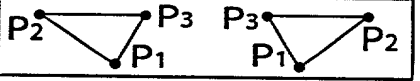
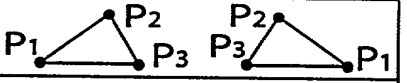
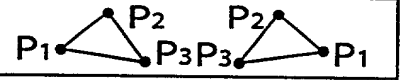
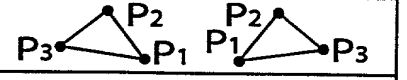
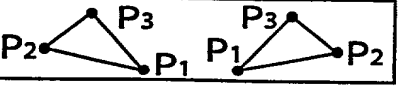
Y_1-Y_2	Y_2-Y_3	Y_1-Y_3	MULTIPLEXER CONTROL	FORM OF TRIANGLE
=	=	=	SORT1	
= = =	= = <	< > =	— — —	
=	<	<	SORT1	
= = =	< > >	> = <	— — —	
=	>	>	SORT5	
<	=	=	—	
<	=	<	SORT1	
< <	= <	> =	— —	
<	<	<	SORT1	
<	<	>	—	
<	>	=	SORT2	
<	>	<	SORT2	
<	>	>	SORT5	
> >	= =	= <	— —	
>	=	>	SORT4	
>	<	=	SORT3	
>	<	<	SORT3	
>	<	>	SORT4	
> >	> >	= <	— —	
>	>	>	SORT6	

FIG.41

	MULTIPLEXER CONTROL					
SORT1	A=P_1	B=P_2	C=P_3	A-B=1-2	A-C=1-3	B-C=2-3
SORT2	A=P_1	B=P_3	C=P_2	A-B=1-3	A-C=1-2	B-C=2-3
SORT3	A=P_2	B=P_1	C=P_3	A-B=1-2	A-C=2-3	B-C=1-3
SORT4	A=P_2	B=P_3	C=P_1	A-B=2-3	A-C=1-2	B-C=1-3
SORT5	A=P_3	B=P_1	C=P_2	A-B=1-3	A-C=2-3	B-C=1-2
SORT6	A=P_3	B=P_2	C=P_1	A-B=2-3	A-C=1-3	B-C=1-2

FIG.42

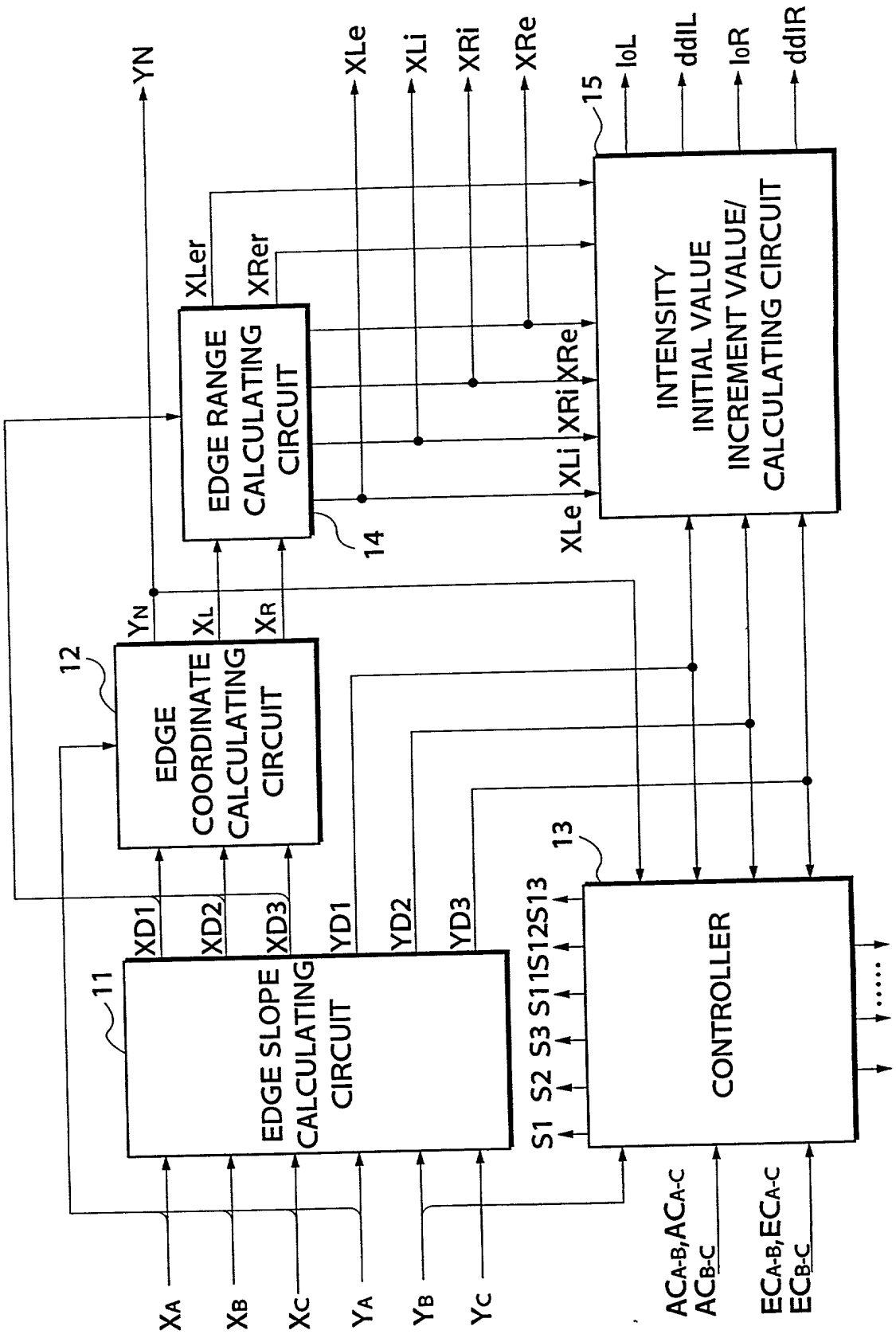

EDGE SLOPE CALCULATING CIRCUIT
11
EDGE COORDINATE CALCULATING CIRCUIT
12
CONTROLLER
13
EDGE RANGE CALCULATING CIRCUIT
14
INTENSITY INITIAL VALUE/ INCREMENT VALUE/ CALCULATING CIRCUIT
15
XD1
XD2
XD3
YD1
YD2
YD3
S1 S2 S3 S11S12S13
YN
XL
XR
XLer
XRer
XLe
XLi
XRi
XRe
IoL
ddIL
IoR
ddIR
XA
XB
XC
YA
YB
YC
ACA-B, ACA-C
ACB-C
ECA-B, ECA-C
ECB-C

FIG.43

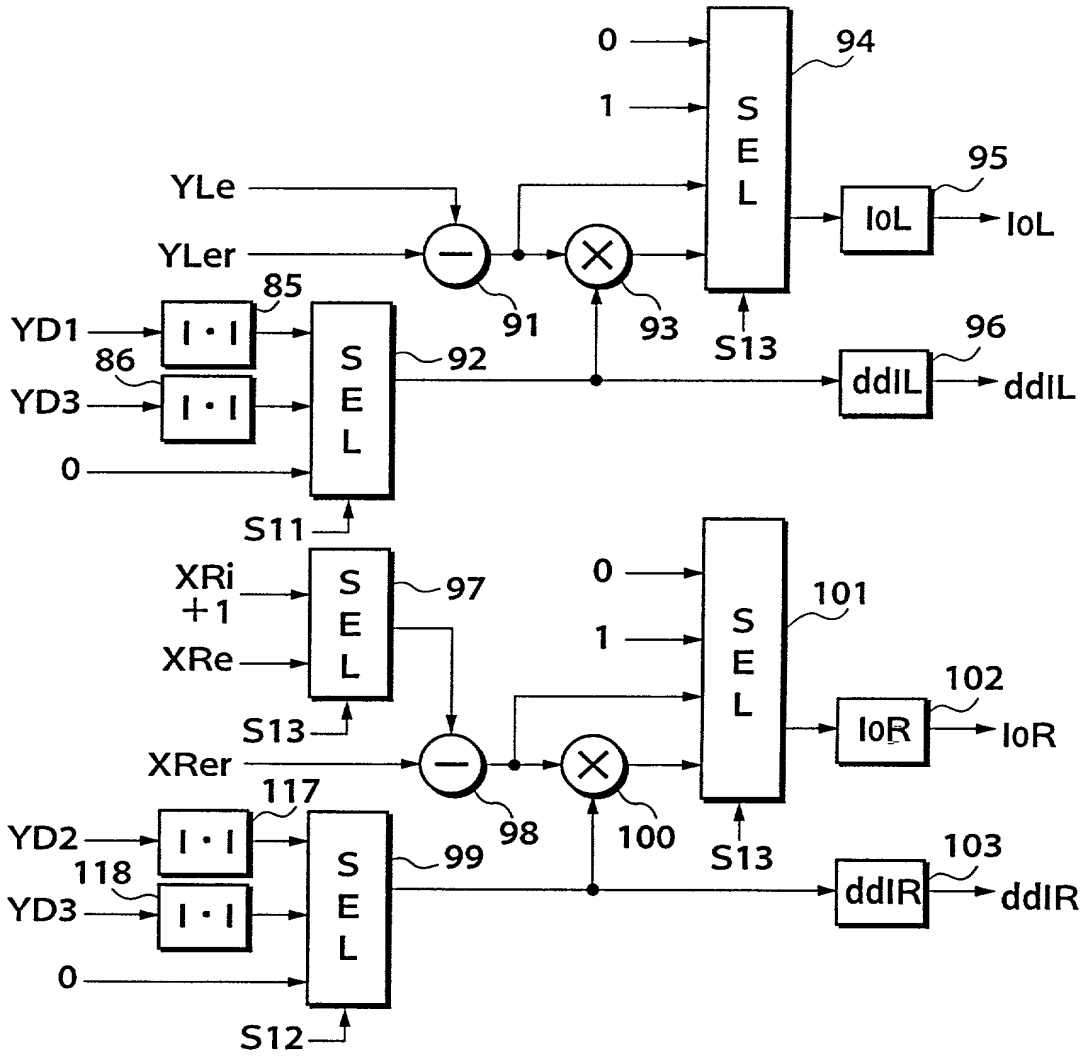
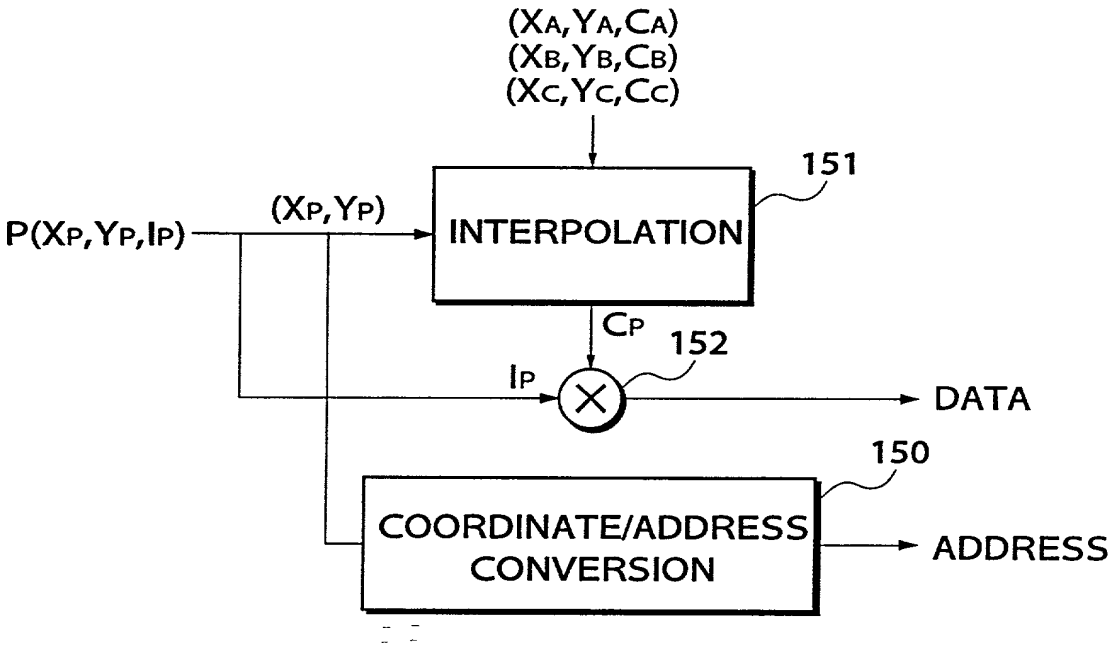

0
1
94
SEL
95
IoL
IoL
YLe
YLer
91
93
S13
85
YD1
I・I
86
YD3
I・I
SEL
92
96
ddIL
ddIL
0
S11
XRi
+1
XRe
SEL
97
S13
0
1
SEL
101
102
IoR
IoR
XRer
98
100
S13
117
YD2
I・I
118
YD3
I・I
SEL
99
103
ddIR
ddIR
0
S12

FIG.44


(XA,YA,CA)
(XB,YB,CB)
(XC,YC,CC)
151
P(XP,YP,IP)
(XP,YP)
INTERPOLATION
CP
152
IP
DATA
150
COORDINATE/ADDRESS CONVERSION
ADDRESS